TsGATE Multiservice Gateway Reference Design

The TsGATE Multiservice Gateway Reference Design combines best-of-breed technologies from Freescale Semiconductor and TeleSoft International. The TeleSoft TsGATE stack is integrated with and ported to the Freescale PowerQUICC II Pro MPC8323E-RDB to create a powerful low cost Integrated Multiservice Reference Design. The software components are designed specifically for embedded solutions and require a minimum of memory space and processor bandwidth. This efficient and cost effective solution has a low cost of manufacture and is ideal for OEMs and ODMs wanting to minimize their technical risks while accelerating time-to-market of their products.

Applications
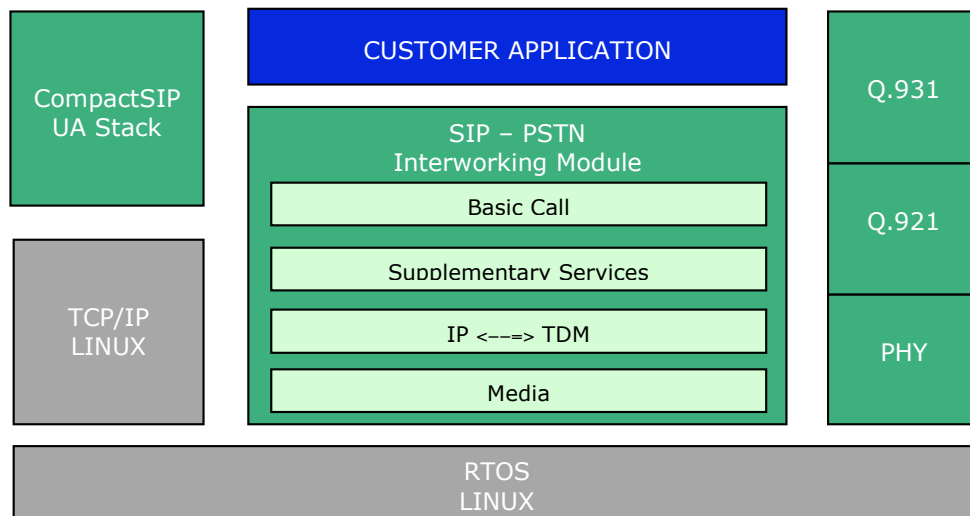Primary applications include Residential Gateways, Multiport ATAs, ML-PPP/Frame Relay/X.25 Gateways.

Features
- Best-of-breed technologies
- Includes SIP-PSTN Signaling
- Optional data protocols
- Fast time-to-market
- Low manufacturing cost
- Single highly integrated processor
- No DSP required
- ANSI C code for easy maintenance

TsGATE
TsGATE is a highly optimized SIP-PSTN stack solution that combines a very small memory footprint for high performance with no compromises on functionality and scalability. CompactSIP's space-efficient operation and superior performance are maximized due to use of handcrafted parsers that avoid typical code bloat caused by parser generators. The Q.931/Q.921/E1/T1/Analog PSTN signaling and data software is available for worldwide applications and has been proven in millions of units deployed.

ISDN (PRI & BRI) signaling is available for worldwide deployment and includes support for all N.America, EuroISDN, Japan, Australia, China and India country variants. QSIG signaling is available for interconnection to PABXs. We also offer 16 country variants for E1 MFC R2 signaling and a comprehensive T1 Robbed-bit stack for N. America.

CompactSIP UA Stack

TCP/IP LINUX

CUSTOMER APPLICATION

SIP – PSTN Interworking Module

Basic Call

Supplementary Services

IP <––=> TDM

Media

Q.931

Q.921

PHY

RTOS LINUX

SOFTWARE BLOCK DIAGRAM

TsGATE conforms to IETF, ITU-T and ECMA standards:

CompactSIP supports 45+ IETF RFCs including:

- RFC 3261 – SIP: Session Initiation Protocol
- RFC 3262 – SIP Reliability (PRACK)
- RFC 3263 – SIP: Locating SIP Servers
- RFC 3264 – SDP Offer/Answer
- RFC 3265 – SIP Specific Event Notification
- RFC 1321 – MD5: Message Digest Algorithm
- RFC 2327 – SDP: Session Description Protocol
- RFC 2617 – HTTP Authentication
- RFC 2806 – URLs for Telephone Calls
- RFC 2833 – RTP Payload for DTMF Dial Digits, Telephone Tones & Telephony Signals

- RFC 2915 – NAPTR: Naming Authority Pointer
- RFC 2976 – SIP INFO Method
- RFC 3204 – MIME Objects for ISUP and QSIG
- RFC 3489 – STUN: Simple Traversal of User Datagram Protocol (UDP) Through NATs
- RFC 3550 – RTP: Real-Time Transport Protocol
- RFC 3515 – SIP Refer Method
- RFC 3581 – SIP Extension for Symmetric Response Routing
- RFC 3665 – SIP Basic Call Flow Examples
- DNS Query/Response

TsGATE is available with any of the following ITU-T PRI, BRI and ECMA QSIG stacks

- Q.931 Worldwide ISDN switch variants
  - N. America NI-1, NI-2, Lucent and Nortel
  - ETSI EuroISDN PRI and BRI
  - Japan INSnet64 and INSnet1500
- Q.921 LAPD & X.25
- QSIG PABX Signaling

- FXS/FXO Analog
- E1 CAS MFC R2 (16 country variants)
- T1 Robbed-bit Signaling
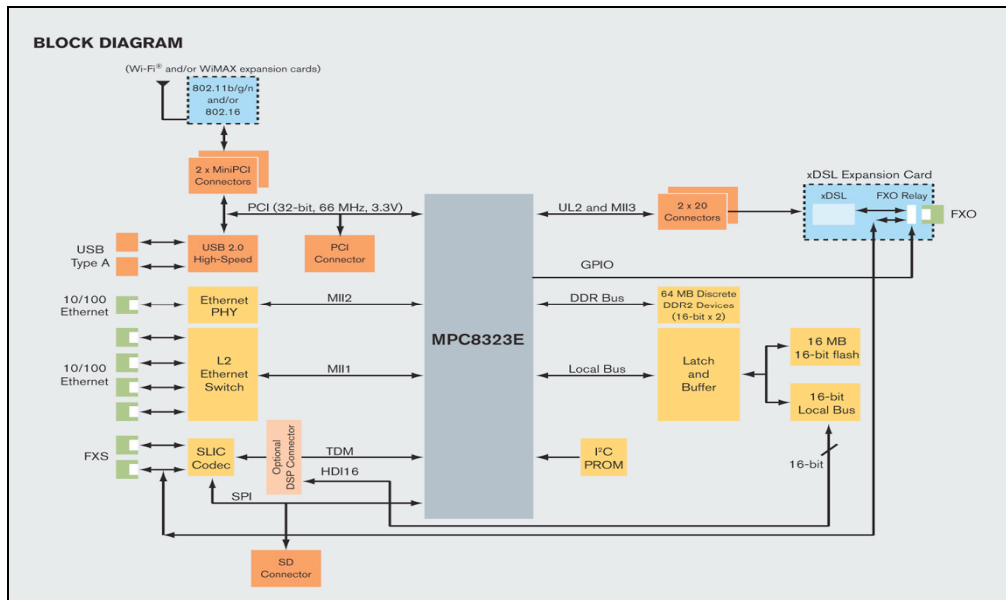- Frame Relay
- ML-PPP
- X.25

TsGATE Interworking Module:

- Compliant with RFC 4497
  - Call setup & teardown between SIP and PSTN

RTOS and TCP/IP

- TsGATE is ported to and runs on Linux version 2.6 RTOS and TCP/IP

TsGATE Gateway Reference Design

The TsGATE Gateway Reference Design is a turnkey hardware/software reference platform supplied with the software of your choice, pre-ported to the platform, in binary and source code form. The binary code provides a running platform that can be used as a base for your final product development. The source code gives you full flexibility and control over your product design, development and support. The TsGATE Gateway Reference Design package includes a complete Hardware Design Kit and Software Source Code Kit. You receive schematics, board layout and component listings, a fully functioning board and source code for the corresponding software.

HARDWARE BLOCK DIAGRAM WITH OPTIONAL MODULES

Note: Information in this datasheet is preliminary and subject to change.

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